REMARKS

Claims 1-29 were previously pending in this application. By this amendment, Applicant is canceling claims 10-21 without prejudice or disclaimer as being directed to non-elected inventions. Claims 1, 22 and 24 are amended and new claims 30-34 are added. As a result, claims 1-9 and 22-34 are pending for examination with claims 1, 22 and 32 being independent claims. No new matter has been added.

Claims Rejections – 35 U.S.C. §102

Claims 1-9 and 22-29 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. patent 6,091,629 to Osada et al. (Osada). Applicant respectfully disagrees.

As an aid to the Examiner, Applicant presents a summary of the specification of the present application and of Osada. This summary is not intended to be a substitute for the Examiner's reading of the Specification and the reference in their entireties. Nor is this summary intended to characterize the invention or any of the terms used in the claims, which are discussed individually below.

Briefly, the present application describes a cache that is useful in a computer system. The cache, because it is implemented with high-speed memory, enables rapid access to information by keeping a copy of information stored in slower-speed memory in the computer system. However, the cache is relatively small, which limits the amount of information that can be available in the cache at one time, creating a need to determine whether a copy of any specific piece of information from the computer system memory is stored in the cache when that information is to be accessed.

To enable a determination of whether information stored at a specific memory address for the computer system is stored in the cache, the cache will frequently be implemented with two components: a data array and a tag array. The data array stores copies of values from a subset of the memory addresses in the computer system. The tag array stores indications of the memory

desirable for many types of computer systems, particularly battery operated devices that use processors.

As described in the Specification and illustrated in FIGs. 7A and 7B, the Applicant has separated the read-process into steps that involve first altering the state of a line in the cache to reflect a bit of information stored in the cache. Separately, the state of that line is sensed with a sense amplifier. The first part of the operation is relatively slow, but consumes little power. The second part of the operation, while relatively fast, consumes a relatively large amount of power. By breaking up the operation in this fashion, the relatively slow, but low power operations may be performed while the tag array is being read. The fast, but high power, parts of the read operation may be performed after the tag array is read. In this way, the data is available quickly but the high-power parts of the read operation may be avoided if the information in the tag array indicates that no copy of the desired information is stored in the data array.

Osada does not describe such a read process. To the contrary, Osada focuses on a write operation for a cache. Of course, there are some similarities between the cache described in Osada and the cache described the present application. For example, both include a tag array and data array. Also, Osada describes that write operations traditionally have been performed in two phases like the read operations described in the present application. In the first phase, a determination is made whether information should be stored in the data array and in the second phase, this information is written to the data array, if it is to be stored.

However, Osada describes a different problem and a different solution than what is described in the present application. Osada describes a problem arising from the need to have two pipeline stages in processor systems that uses a cache in order to accommodate the two phases of a cache write operation. Because the power consumed by a processor may be related to the number of pipeline stages, a cache that requires two pipeline stages for write operations causes an overall increase in the power consumed by the processor (see, e.g., col. 2, lines 16-21).

To address this problem, Osada proposes an architecture for the data array that replaces a line, to which a memory cell is connected, with three separate lines. For example, FIG. 1 illustrates a memory cell (CELL). Those three separate lines are identified as a local bit line (comprising the pair LBL and LBLB), a global read line (consisting of the pair RGBL and RGBLB) and global write line (consisting of the pair WGBL and WGBLB). The local bit line, because it is connected directly to the memory cell, must be used for either a read or a write operation involving the cell. However, the global read and write lines are connectable to the cell through switches, labeled MN5, MN6, MP3 and MP4. With this configuration, the global read lines can be precharged in preparation for a read operation, even though not connected to the cell. Likewise, the global write lines can be charged with a value representing new data to be written to the cell, even though not connected to the cell. The global read lines or write lines can then, through the use of the switching transistors MN5, MN6, MP3 and MP4, be quickly connected to a cell to complete a read or write operation.

This configuration is useful if read and write operations alternate. With this configuration, a read operation can be performed, using the global read line and local line while the global write line is being prepared for the next write operation. Conversely, during a write operation using the global write line and the local line, the global read line can be prepared for a subsequent read operation.

FIG. 8 of Osada illustrates how this capability to rapidly perform alternating read and write operations can be used to avoid the need for an additional pipeline stage in a system using a cache. During a memory write operation, the address to be written is applied to the cache. Initially, data at a location in the cache corresponding to the applied address is read and stored in a recovery buffer (114). This read operation can be performed using the global read line while the global write line is being prepared to write the data into the same location in the data array. Accordingly, once the information is read from the cache data array and stored in the recovery buffer, the global write line is ready to begin a write operation to store information in the cache data array location. Both of these steps can be performed while the tag array (113) is being accessed to determine whether the data applied to the cache should be stored in the data array. If, as a result of reading data from the cache tag array, a determination is made that the information should be stored

in the cache data array, the write operation may be regarded as complete because the new data has already been written into the data array. However, if the information read from the tag array indicates that the value should not have been stored in the cache data array, the data already written in the data array should not have been stored in the cache and data from the recovery buffer is written back into the cache data array, restoring the desired value.

No part of Osada deals with avoiding the use of a sense amplifier to read the cache data array based on information stored in the tag array. To the contrary, the process described in Osada increases the number of times that the sense amplifier for the cache data array is used. As described, every write access to the cache tag array involves a read operation using the sense amplifier.

The differences in the purpose and steps of the processes described in Osada and in the present application are reflected in the claims. For example, claim 1 recites: "selectively altering the state of at least one line in the way in the data array . . . starting before completing the determination" in combination with "selectively enabling at least one sense amp associated with the at least one line in the way in the data array." Further, the claim makes clear that the selective enabling occurs "after completing the determination" and "when the information indicates an item is stored in the way in the data array." Osada does not teach or suggest a process meeting these limitations of the claim.

The Examiner asserts that Osada, in describing writing data before establishing a hit signal, teaches altering the state of a line before completing the determination as recited in element b) of claim 1. However, element b) recites that the altering is "based on a value stored in at least one cell of the way of the data array." Accordingly, the write portion of the operation described in Osada does not meet this limitation.

The Examiner also asserts that col. 6, lines 50-53 of Osada meets the limitations in element c) relating to "selectively enabling at least one sense amp." Applicants respectfully disagree with the Examiner's interpretation of Osada. Column 6, lines 50-53 describes turning on a

specific enable signal only when the global bit lines are amplified as a way to reduce power consumption. As understood, these passages describe the specific mechanisms by which a sense amplifier may be enabled. They do not relate to the times at which the amplifier should be enabled. Accordingly, the cited passages are unrelated to the claimed elements.

The Examiner also rejects independent claim 22 based on the same passages of Osada. However, the write operation described in Osada does not meet limitations of the claim, such as: "altering the state of lines associated with the first portion of the applied address . . . with the state of the lines based on information stored in the data array," as recited by the claim.

The Examiner also cites column 6, lines 50-55 as teaching the claimed time for sensing the state of a line, as recited in claim 22. However, as noted above, that passage does not describe the times at which the sense amp is enabled and the reference therefore does not teach or suggest limitations of the claim, such as: "after the first time, sensing the state of a line associated with the first portion of the applied address in the data array, with the sensed line selected in response to the indication of a match."

Claims 2 through 9 and 23 through 29 depend, either directly or indirectly, from one of claims 1 or 22. Accordingly, each of the dependent claims distinguishes the reference for at least the reasons given above. Additionally, the dependent claims recite limitations that further distinguish the reference. For example in conjunction with claim 3, the Examiner asserts that it is known to provide the output of the sense amp as an output of the cache. However, the relevant question is whether the limitations of claim 3, including all of the limitations of claim 1, are shown or suggested in the reference. In Osada, the read operation described is a stage of a write operation, designed to provide a value for recovery buffer (114). Accordingly, the values read during the write operation that is the subject of Osada are not output and do not meet the limitations of claim 3.

New claims 30 through 33 likewise distinguish the references. New claims 30 and 31 depend from claim 1 and recite further details of the method of claim 1 that are not shown or suggested in Osada. New claim 32 recites a method of performing a read operation with a cache.

The claim recites actions during a first interval and actions during a second interval. During the first interval, the state of a line is altered by connecting a selected cell to the line. During a second interval, based on determination made in the first interval, the sensing amp is selectively enabled. Accordingly, the newly added claims recite limitations not shown or suggested in Osada.

Because each of the claims recites one limitation not shown or suggested in the reference, the rejection should be withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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